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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 14, 2007 — Jennifer A. Steele

Date — Jennifer A. Steele

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Timothy B. Cowles, Michael A. Shore and Patrick J. Mullarkey	Attorney Docket No.:	500792.03
Patent No.	: US 6,925,021 B2	Serial No.	: 10/043,680
Issue Date	: August 2, 2005	Filed	: January 10, 2002
Title	: REFRESH CONTROLLER AND ADDRESS REMAPPING CIRCUIT AND METHOD FOR DUAL MODE FULL/REDUCED DENSITY DRAMS		

NOTIFICATION OF ERRORS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
FEB 26 2007
of Correction

Sir:

The following errors were noted in a review of the above-identified letters patent. One or more of these errors was inadvertently made in the original application, while the others occurred in the printing of the patent. Since the errors are of an obvious nature, a formal Certificate of Correction is not believed to be warranted at this time. Therefore, applicants request that this notification be placed in the Patent and Trademark Office file.

Column, Line	Reads	Should Read
Item (75) Inventors	"Timoty B. Cowles,"	--Timothy B. Cowles,--
Item (57), Line 19	"with system adapted"	--with systems adapted--
Column 1, Line 10	"field Mar. 8, 2001,"	--filed Mar. 8, 2001,--

Column 1, Line 38	"memory cell in an"	--memory cell in--
Column 1, Line 47	"or decreased"	--or decrease--
Column 1, Line 57	"in the art. DRAM memory"	--in the art, DRAM--
Column 2, Line 3	"logic level of can no longer"	--logic level can no longer--
Column 2, Line 6	"example, as a result"	--example, a result--
Column 2, Line 15	"problems is disclosed"	--problem is disclosed--
Column 2, Line 12	"to redirected memory"	--to redirect memory--
Column 2, Line 23	"complimentary"	--complementary--
Column 2, Line 26	"to store in"	--to store--
Column 2, Line 55	"i.e., **11** row address"	--i.e., 11 row address--
Column 2, Line 67	"limitations of DRAM's"	--limitations of DRAMs--
Column 3, Line 2	"of such DRAM's."	--of such DRAMs.--
Column 3, Line 13	"command are applied"	--commands are applied--
Column 3, Line 52	"half density mode,"	--half-density mode,--
Column 4, Line 9	"receiving a time-"	--receiving time- --
Column 4, Line 36	"signals applied the"	--signals applied to the--
Column 4, Line 39	"from the Memory Address"	--from the memory address--
Column 4, Line 40	"corresponding Row Address"	--corresponding row address--
Column 4, Line 57	"WL**0**-WLN in a"	--WL**0**-WLN in an--
Column 4, Line 59	Raz in a well known"	--RAz in a well-known--
Column 5, Line 6	"Raz in a well known"	--RAz in a well-known--
Column 5, Line 9	"RA**0**, . . . , Raz."	--RA**0**, . . . Raz.--
Column 5, Line 15	"for clarity, it will be"	--for clarity. It will be--
Column 5, Lines 27 and 44	"multitude of complimentary"	--multitude of complementary--
Column 5, Line 39	"then energized"	--then energizes--

Column 6, Line 26	"from the Memory Address"	--from the memory address--
Column 6, Line 27	"corresponding Row Address"	--corresponding row address--
Column 6, Lines 45 and 67	"complimentary"	--complementary--
Column 7, Lines 5 and 8-9	"complimentary"	--complementary--
Column 7, Lines 7, 37 and 50	"compliment"	--complement--
Column 7, Line 39	"voltages on the both digit"	--voltages on both the digit--
Column 7, Line 41	"only one digit lines"	--only one digit line--
Column 7, Lines 59-60	"each Memory Address"	--each memory address--
Column 8, Line 7	"one of the row address"	--one of the row addresses--
Column 8, Lines 40 and 54	"complimentary"	--complementary--
Column 8, Line 57	"is operates"	--operates--
Column 9, Line 23	"is increment half"	--is incremented half--
Column 9, Lines 49 and 51	"one-eight"	--one-eighth--
Column 10, Line 52	"compliment"	--complement--
Column 10, Line 55	"thereby applying causing an"	--thereby causing an--
Column 11, Line 32	"row address"	--row addresses--
Column 11, Line 34	"SDRAMS"	--SDRAMs--
Column 11, Line 36	"address buffen"	--address buffer--
Column 11, Line 38	"address bids"	--address bits--
Column 11, Line 50	"signifficant"	--significant--
Column 11, Line 66	"SDKAM **20**"	--SDRAM **20**--
Column 12, Line 40	"stages the first of which"	--stages, the first of which--

Column 12, Line 41	"the second stage of the being"	--the second stage being--
Column 12, Line 45	"circuit coupled the first"	--circuit coupled to the first--
Column 12, Line 66	"store a colunm"	--store a column--
Column 13, Line 9	"being enable responsive"	--being enabled responsive--
Column 13, Line 36	"second stages the first"	--second stages, the first--
Column 13, Line 41	"circuit coupled the first"	--circuit coupled to the first--
Column 14, Line 13	"being enable responsive"	--being enabled responsive--
Column 14, Line 41	"second stages the first"	--second stages, the first--
Column 14, Line 46	"circuit coupled the first"	--circuit coupled to the first--

Respectfully submitted,

Date: Feb. 12, 2007

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Enclosure:
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